USN | | | | | | | | | | |

06EC62

Sixth Semester B.E. Degree Examination, June/July 2011

Microprocessors

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions, selecting at least TWO questions from each part.***
2. ***Missing data be suitably assumed.***

PART – A

1 a. Explain the "look ahead" features of 8086 processor. **(08 Marks)**

b. With suitable examples, explain PSW in 8086 processor. **(06 Marks)**

c. The opcode for MOV instruction is 100010. Determine the machine language code for the following instructions :

i) MOV AL, BL ii) MOV, AX, BX
iii) MOV AL, [BX] iv) MOV AX, DS : [BP + SI]
v) MOV AL, [1234h] vi) MOV AL, 34h [BX] [DI] **(06 Marks)**

2 a. Determine whether the following instructions are valid or not. If valid, explain their operation and flags affected, if not valid mention the reason :

i) XLAT AL ii) MOV BX, [DX]
iii) NOT 34h iv) AAD
v) TEST OPR1, OPR2 vi) JNGE label. **(06 Marks)**

b. Write a program to check whether the given string is palindrome or not. Accept the string through keyboard and print a suitable message, as "PALINDROME" or "NOT PALINDROME". **(06 Marks)**

c. What are assembler directives? Explain the significance of the following assembler directives with suitable examples:

i) LENGTH ii) TYPE iii) DB iv) EQU **(08 Marks)**

3 a. List the string primitives. Explain them with suitable examples. **(08 Marks)**

b. Write 8086 MACRDs to accept a data from keyboard and to display result on CRT screen. Using above macros, write a program to add two unpacked BCD numbers. **(06 Marks)**

c. Write an algorithm and a program to convert the given four digit BCD data to its equivalent Hexadecimal value. **(06 Marks)**

4 a. Explain the interrupt structure of 8086. Write the functions of atleast five dedicated software interrupts in 8086. **(08 Marks)**

b. Write a scheme to generate NMI interrupt on power failure and explain. **(06 Marks)**

c. Write subroutines to perform the following in 8086 processor :

i) Set trap flag
ii) Reset trap flag **(06 Marks)**

PART – B

5 a. With relevant interface diagrams, write a flowchart and program code for 4 × 4 matrix keyboard detect, debounce and encode procedure. **(10 Marks)**

b. Write an algorithm and a program for an 8086 procedure to drive the stepper motor. Assume the desired direction of rotation is passed to the procedure in AL (AL = 1 is clockwise, AL = 0 is counter-clockwise) and the number of steps is passed to the procedure in CX. Also assume full-step mode and the delay of 20 ms between each step. Show the necessary interfacing details. **(10 Marks)**

6 a. Represent 178.625 using 80 bit temporary real format. Use hex format for expressing the answer. **(04 Marks)**

b. Explain the following instructions of 8087 coprocessor with suitable examples :
i) FILD ii) FXCH iii) FLDPI iv) FINIT **(08 Marks)**

c. Draw the formats of STATUS and CONTROL registers of 8087 NDP and define each bit. **(08 Marks)**

7 a. Draw a timing diagram to execute a memory write operation in minimum mode of 8086 processor and explain. **(06 Marks)**

b. What are the different status that are given out on the bus $\overline{S}_2$, $\overline{S}_1$ and $\overline{S}_0$ in maximum mode of 8086? How different control signals are generated from this bus? Explain briefly each of these control signals. **(08 Marks)**

c. Explain the operation of reset section of 8284A clock generator. **(06 Marks)**

8 a. Explain the function of the following 80386 pins :
i) $\overline{\text{ERROR}}$ ii) $\overline{\text{PEREQ}}$ iii) $\overline{\text{LOCK}}$ iv) $\overline{\text{READY}}$
v) $\overline{\text{ADS}}$ vi) RESET vii) D / $\overline{\text{C}}$ viii) $\overline{\text{NA}}$ **(08 Marks)**

b. Write a note on the internal programming model of the 80486 and depict the EFLAG register in detail. **(07 Marks)**

c. Explain the following with respect to Pentium processor :
i) Branch prediction logic
ii) Cache structure
iii) Super scalar architecture. **(10 Marks)**

* * * * *